

भारतीय प्रौद्योगिकी संस्थान तिरुपति

Indian Institute of Technology Tirupati Renigunta Road, Settipalli Post, Tirupati – 517506

Telephone: 0877-2503572, Email: purchase@iittp.ac.in

Tender No. IITT/ ELE/2022-23/22

18 May 2022.

NOTICE INVITING TENDER FOR SUPPLY, INSTALLATION, TESTING AND COMMISSIONING OF DATA ACQUISITION SYSTEM

(E-PROCUREMENT MODE ONLY)

Indian Institute of Technology Tirupati (IIT Tirupati) invites online bids (e-tender) in Two bid system from eligible Class-I & Class-II in line with Government Public Procurement order No.P-45021/2/2017-BE-II dated: 04.06.2020 for the following:

Item Description	Quantity (approx.)	Tender Fee (Inclusive of all taxes in Rs.)
Supply, installation, testing and commissioning of Data Acquisition System as per the specifications of the tender documents	01 No.	500/-
Total		500/-

The Tender Document can be downloaded from Central Public Procurement (CPP) Portal http://eprocure.gov.in/eprocure/app and bid is to be submitted online only through the same portal up to the last date and time of submission of tender.

Critical Dates of Tender:

1	Date and time of Online Publication/Download of Tenders	18.05.2022	18.00 hrs
2	Bid submission start date & time	18.05.2022	18.00 hrs
3	Bid submission close date & time	08.06.2022	15.00 hrs
4	Closing date & time for submission of EMD/Tender fee	08.06.2022	15.00 hrs
5	Opening of Technical bids	09.06.2022	15.00 hrs

1. About IIT TIRUPATI:

Indian Institute of Technology Tirupati (IIT Tirupati) is an Autonomous Institute under Ministry of Education, Govt. of India.

2. Technical Specifications: Schedule of requirement

S.No	Item Description w	vith Specifications		
1	DATA ACQUISIT	TION SYSTEM -01 No.		
	The required Specifications for the Data Acquisition System have been given below:			
	Analog Input	Number of channels 4 differential ADC resolution 16 bits DNL No missing codes INL Refer to the AI Absolute Accuracy section. Sample rate (simultaneous sampling on all channels sampled) Maximum 3.571 MS/s Minimum No minimum Timing resolution 10 ns Timing accuracy 50 ppm of sample rate Input coupling DC Input range ± 1 V, ± 2 V, ± 5 V, ± 10 V Maximum working voltage for all analog inputs Positive input (AI+) ± 11 V for all ranges, Measurement Category I Negative input (AI-) ± 11 V for all ranges, Measurement Category I Caution Do not use for measurements within Categories II, III, and IV. CMRR (at 60 Hz) 75 dB Bandwidth 1 MHz THD - 80 dBFS Input impedance Device on AI+ to AI GND > 100 G Ω in parallel with 100 pF AI- to AI GND > 100 G Ω in parallel with 100 pF AI- to AI GND 2 k Ω Input bias current ± 10 pA Crosstalk (at 100 kHz) Adjacent channels - 80 dB Non-adjacent channels - 100 dB Input FIFO size 8 ,182 samples shared among channels used Data transfers DMA (scatter-gather), programmed I/O Overvoltage protection for AI < 03 >, APFI 0 Device on ± 36 V Device off ± 15 V Input current during overvoltage conditions ± 20 mA max/AI pin		

	Number of triggers 1
	Source AI <03>, APFI O Functions Start Trigger, Reference Trigger, Pause
	Trigger, Sample Clock, Sample Clock Timebase
	Source level
	AI <03> ±Full scale
	APFI 0 ±10 V
	Resolution 16 bits
	Modes Analog edge triggering, analog edge triggering
	with hysteresis, and analog window triggering
Analog Triggers	Bandwidth (-3 dB)
	AI <03> 3.4 MHz
	APFI 0 3.9 MHz
	Accuracy ±1% of range
	APFI O characteristics
	Input impedance 10 k Ω
	Coupling DC
	Protection, power on ±30 V
	· ·
	Protection, power off ±15 V
AI Absolute Accuracy	Gain tempco 8 ppm/°C
(Warranted)	Reference tempco 5 ppm/°C Residual offset error 15 ppm of range
(Trained)	INL error 46 ppm of range
	Number of channels 2
	DAC resolution 16 bits
	DNL ±1 LSB, max
	Monotonicity 16 bit guaranteed
	Accuracy Refer to the AO Absolute Accuracy section Maximum update rate
	(simultaneous)
	1 channel 3.3 MS/s
	2 channels 3.3 MS/s
	Minimum update rate No minimum
	Timing accuracy 50 ppm of sample rate
	Timing resolution 10 ns
	Output range ±10 V, ±5 V, ±external reference on APFI 0
	Output coupling DC
Analog Output	Output impedance 0.4 Ω
Allaiog Gatpat	Output current drive ±5 mA
	Overdrive protection ±25 V
	Overdrive current 10 mA
	Power-on state ±5 mV
	Power-on/off glitch 1.5 V peak for 200 ms
	·
	Output FIFO size 8,191 samples shared among channels used
	Data transfers DMA (scatter-gather), programmed I/O
	AO waveform modes Non-periodic waveform, periodic waveform regeneration
	mode from onboard FIFO, periodic waveform regeneration from host buffer
	including dynamic update
	Settling time, full-scale step, 15 ppm (1 LSB) 2 μs
	Slew rate 20 V/μs
	Glitch energy at midscale transition, ±10 V range 6 nV · s

1	
External Reference	APFI 0 characteristics Input impedance 10 k Ω Coupling DC Protection, device on ± 30 V Protection, device off \pm 15 V
	Range ±11 V Slew rate ±20 V/μs
AO Absolute Accuracy (Warranted)	Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.
Digital I/O/PFI	Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 k Ω typical, 20 k Ω minimum Input voltage protection ±20 V on up to two pins
Waveform Characteristics (Port 0 Only)	Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable
PFI/Port 1/Port 2 Functionality	Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input
Recommended Operating Conditions	Input high voltage (VIH) Minimum 2.2 V Maximum 5.25 V Input low voltage (VIL) Minimum 0 V Maximum 0.8 V Output high current (IOH) P0.<07> -24 mA maximum PFI <015>/P1/P2 -16 mA maximum Output low current (IOL) P0.<07> 24 mA maximum PFI <015>/P1/P2 16 mA maximum
Digital I/O Characteristics	Positive-going threshold (VT+) 2.2 V maximum Negative-going threshold (VT-) 0.8 V minimum Delta VT hysteresis (VT+ - VT-) 0.2 V minimum IIL input low current (VIN = 0 V) -10 µA maximum IIH input high current (VIN = 5 V) 250 µA maximum

1	
Timing I/O	Number of counter/timers 4 Resolution 32 bits Counter measurements Edge counting, pulse, pulse width, semiperiod, period, two-edge separation Position measurements X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding Output applications Pulse, pulse train with dynamic updates, frequency division equivalent time sampling Internal base clocks 100 MHz, 20 MHz, 100 kHz External base clock frequency 0 MHz to 25 MHz Base clock accuracy 50 ppm Inputs Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock Routing options for inputs Any PFI, RTSI, analog trigger, many internal signals FIFO 127 samples per counter Data transfers Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O
Frequency Generator	Number of channels 1 Base clocks 20 MHz, 10 MHz, 100 kHz Divisors 1 to 16 Base clock accuracy 50 ppm
Phase-Locked Loop (PLL)	Number of PLLs 1 Output of PLL 100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases
External Digital Triggers	Source Any PFI, RTSI Polarity Software-selectable for most signals Analog input function Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase Analog output function Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase Counter/timer functions Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock Digital waveform generation (DO) function Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase Digital waveform acquisition (DI) function Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Device-to-Device Trigger Bus	Input source RTSI <07> Output destination RTSI <07> Output selections 10 MHz Clock, frequency generator output; many internal signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input
Bus Interface	Form factor x4 PCI Express, specification v1.1 compliant Slot compatibility x4, x8, and x16 PCI Express slots DMA channels 7 DMA, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3
Power Requirements	3.3 V 4.0 W and 12 V 13.2 W
Current Limits	5 V terminal (connector 0) 1 A maximum2 P0/P1/P2/PFI terminals combined 1.4 A maximum

Spares and Service	Minimum 5 years
Warranty	Three Years Onsite warranty.
Required Accessories	EPM Shielded Cable, 68-D-Type to 68 VHDCI Offset, 2 m BNC-2110 Noise Rejecting, Shielded BNC Connector Block -1Quantity And All required accessories.
Storage Environment	Ambient temperature range -20 °C to 70 °C Relative humidity range 5% to 95% RH, noncondensing SCB-68A Noise Rejecting, Shielded I/O Connector Block -1Quantity SHC68-68
Operating Environment	Operating temperature, local 0 °C to 50 °C Operating humidity 10% to 90% RH, noncondensing System slot airflow 0.4 m/s (80 LFM)
Environmental Maximum altitude 2,000 m (800 mbar) (at 25 °C ambient temperature Pollution degree 2	
Safety Voltages	Channel-to-earth ground ±11 V, Measurement Category I
Calibration	Recommended warm-up time 15 minutes Calibration interval 2 years
Physical	Weight 110 g (4.0 oz) I/O connectors PCIe device connector 68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle) Cable connector 68-Pos Offset IDC Cable Connector (Plug) (SHC68-*) Form factor Standard height, half length, single slot Integrated air mover (fan) No

- All offered products technical Specifications and Brochures are to be submitted along with the Technical Bid.
- The detailed scope of coverage of Warranty shall be provided in the compliance statement -Annexure-VII.
- The Bidder shall furnish, as part of its bid, documents establishing the conformity of the Equipment that the Bidder proposes to supply under the Contract to the requirements of the Purchaser, as given in the Tender Document.
- The documentary evidence of conformity of the Equipment to the Tender Document may be in the form of written descriptions supported by Brochure / literature / diagrams / certifications, including: (a) A detailed description of the essential technical, functional and performance characteristics of the Equipment that the Bidder is proposing to supply; (b) Technical details of the major subsystems/components of the Equipment.

3. TENDER FEE & BID SECURITY DECLARATION DETAILS:

- **3.1 Tender Fee of Rs.500/- (Rupees five hundred only)** should be submitted through ECS (Bank transfer / NEFT / RTGS) in favour of <u>Indian Institute of Technology Tirupati</u>.
- 3.2 Bank A/c Details for crediting Tender Fee:

Name : Indian institute of Technology Tirupati Main Account

Bank : State Bank of India

Account No : 35523338208 IFSC Code : SBIN0006677

3.3 Tender Fee and Bid Security Exemption:

I) Micro and Small Enterprises (MSEs):

Micro and Small Enterprises (MSEs) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME) **for goods produced and services rendered**, are exempted from Tender fee and Bid Security. However, they have to enclose **valid self-attested registration certificate(s)** along with the tender to this effect.

Accordingly, MSEs shall be required to submit valid **Udyam Registration Certificate** for availing benefit under MSE Procurement Policy.

The benefit as above to MSEs shall be available only for Goods produced and services rendered by MSEs. However, traders are excluded from the purview of MSE Procurement Policy.

II) Startup(s):

Startup(s) as recognized by **Department for Promotion of Industry and Internal Trade (DPIIT)**, Govt. of India, are exempted from Tender fee and Bid Security. However, they have to enclose *valid self-attested registration certificate(s)* along with the tender to this effect.

Eligible MSE and startup bidders who seeks exemption from Tender fee/Bid Security as per clause no. (c) above, if they withdraw or modify their bids during the period of validity, or if they are awarded the contract and they fail to sign the contract, or to submit a performance security before the deadline defined in the request for bids document, they will be suspended for the period of three years or as decided by the competent authority from being eligible to submit bids for contracts with the entity that invited the bids.

- **3.4** The Bidders will have to upload scanned copy of Payment details towards tender fee and the same will be accepted only on verification and confirmation by the Institute. Any delay in credit will not be entertained by the Institute. (**As per the format attached in Annexure I**)
- 3.5 Other than eligible MSE and Startup bidders, Bid Security Declaration:

Bidders should have to submit the Bid Security Declaration (As per the format attached in annexure-II) in duly filled and signed condition.

4. ELIGIBILITY CRITERIA

4.1 Other Important Documents (OIDs)

Firm Incorporation Certificate, PAN details, GST details are to be provided.

4.2. Statutory Documents:

- I) The Bidder should give self-declaration certificate for acceptance of all terms & conditions of tender documents. A duly completed certificate to this effect is to be submitted as per the Annexure-I.
- II) The firm should not be in the active debarred list by any Central / State Government / Public Undertaking / Institute and no criminal case registered / pending against the firm or its owner / partners anywhere in India. A duly completed certificate to this effect is to be submitted as per Annexure-III.

III) Experience and Past Performance:

The bidder/OEM should have supplied similar system during past three financial years **i.e. during 2017-18 to 2019-20 or 2018-19 to 2020-21** in India to Central / State Govt/ PSU/ CPSEs/ Educational R&D Institutions. Vendor should provide satisfactory installation certificates with product details as proof with customer contacts email and phone number as per the **Annexure-IV**.

- IV) The Annual Turnover should be at least Rs. 1 Lakh and be profitable during each of the previous three financial years i.e. during 2017-18 to 2019-20 or 2018-19 to 2020-21. Audited financial Statements or Financial Statements showing turnover duly signed by a Chartered Accountant are to be submitted as per the Annexure-V.
- V) In case the bidder is a <u>Class-I / Class-II</u> in line with the Public Procurement (Preference to Make in India) Order 2017 No. P-45021/2/2017-PP (BE-II) dated 04 Jun 2020 as amended from time to time. A Self-Declaration Certificate regarding "Class-I/Class-II Supplier" for the tendered items as per the Annexure-VI is to be submitted.

As per the OM of Department of Promotion for Industry and Internal Trade No. P-45021/102/2019-BE-II-Part(1) dated: 04.03.2021. The bidders can't claim themselves as Class-I local suppliers/Class-II local suppliers by claiming the services such as transportation, insurance, installation, commissioning, training and after sales service support like AMC/CMC etc. as local value addition.

a. 'Local Content' means the amount of value added in India which shall, unless otherwise prescribed by the Nodal Ministry, be the total value of the

- item procured (excluding net domestic indirect taxes) minus the value of imported content in the item (including all custom duties) as a proportion of the total value, in percent.
- b. 'Class-I local supplier' means a supplier or service provider, whose goods, services or works offered for procurement, has local content equal to or more than 50% as defined under this order.
- c. 'Class-II local supplier' means a supplier or service provider, whose goods, services or works offered for procurement, has minimum local content of 20% but less than 50%, as defined under this order.
- d. 'Non-local supplier'means a supplier or service provider, whose goods, services or works offered for procurement, has local content less than 20%, as defined under this order.
- e. Complaint redressal mechanism: In case any complaint received by the procuring agency or the concerned Ministry/Department against the claim of a bidder regarding local content/domestic value addition in an electronic product, the same shall be referred to STQC.
- f. The bidder shall be required to furnish the necessary documentation in support of the domestic value addition claimed in an electronic product to STQC. If no information is furnished by the bidder, such laboratories may take further necessary action, to establish the bonafides of the claim.
- g. A complaint fee of Rs. 2 lakh or 1% of the value of the domestically manufactured products being procured (subject to a maximum of Rs.5 lakh), whichever is higher, to be paid by Demand Draft to be deposited with STQC. In case, the complaint is found to be incorrect, the complaint fee shall be forfeited. In case, the complaint is upheld and found to be substantially correct, deposited fee of the complainant would be refunded without any interest.
- h. False declarations will be in breach of the Code of Integrity under Rule 175 (1)(i)(h) of the General Financial Rules for which a bidder or its successors can be debarred for up to two years as per Rule 151 (iii) of the General Financial Rules along with such other actions as may be permissible under law.
- VI) The bidder should be OEM or OEM authorized Dealers / Channel partners / Distributors of reputed brand having authorization for sales and after sales support. Valid OEM authorization letter is required to participate in this tender.

VII) Prior Registration and / or Screening of bidders:

Any bidder from a country which shares a land border with India will be eligible to bid in this tender only if the bidder registered with the competent authority. The concerned bidder(s) are required to attach the relevant valid Registration Certificate along with the bid for consideration.

"Bidder" (including the term 'tenderer', consultant or service provider in certain contexts) means any person or firm or company, including any member of a consortium or joint venture (that is an association of several persons, or firms or companies), every artificial juridical person not falling in any of the descriptions of bidders stated hereinbefore, including any agency branch or office controlled by such person, participating in a procurement process.

"Bidder from a country which shares a land border with India" for the purpose of this Order means :-

- An entity incorporated, established or registered in such a country; or
- A subsidiary of an entity incorporated, established or registered in such a country or
- An entity substantially controlled through entities incorporated, established or registered in such a country; or
- An entity whose beneficial owner is situated in such a country; or
- An Indian (or other) agent of such an entity; or
- A natural person who is a citizen of such a country; or
- A consortium of joint venture where any member of the consortium or joint venture falls under any of the above.

The detailed terms & conditions issued from time to time in this regard by Government of India will be applicable.

VIII) Authorized Representatives:

Bids of bidders quoting as authorised representative of a principal manufacturer would also be considered to be qualified, provided:

- (i) Their principal manufacturer meets all the criteria above without exemption, and
- ii) The principal manufacturer furnishes a legally enforceable tender-specific authorisation assuring full guarantee and warranty obligations as per the general and special conditions of contract;

and

iii) The bidder himself should have been associated, as authorised representative of the Principal Manufacturer for same set of services as in present bid (supply, installation, satisfactorily commissioning, after sales service as the case may be) for same or similar item for past three years ending on bid opening date.

4.3 TECHNICAL CRITERIA

Bidders should comply the specification of the tendered item in all respect. The detailed format is attached at Annexure-VII. The bidder is to complete the same in all respect and submit accordingly

5. FINANCIAL BID DETAILS

- 5.1 Financial bid i.e. BOQ given with tender (in **Excel format**) to be downloaded first and uploaded after filling all relevant information strictly as per the format failing which the offer is liable for rejection. Kindly quote your offer on FOR IIT Tirupati (inclusive of all taxes and charges). **Vendor should quote prices in BOQ only, offers indicating rates anywhere else shall be liable for rejection.**
 - 5.2 Concessional Custom Duty / Concessional GST is applicable to IIT Tirupati as a Research Institution. Necessary Certificate to this effect shall be provided by IIT Tirupati to the supplier.

6. TIME SCHEDULE:

S. No.	Particulars	Date	Time
a.	Date of Online Publication of Tender	18.05.2022	18.00 hrs
b.	Bid Submission Start Date	18.05.2022	18.00 hrs
c.	Bid Submission Close Date	08.06.2022	15.00 hrs
d.	Closing Date & Time for Submission of EMD & Tender Fee	08.06.2022	15.00 hrs
e.	Opening of Technical Bids	09.06.2022	15.00 hrs

7. AVAILABILITY OF TENDER

The tender document can be downloaded from http://eprocure.gov.in/eprocure/app and be submitted only through the same website.

8. BID VALIDITY PERIOD

The bid will remain valid for 90 days from the date of opening as prescribed by IIT Tirupati. A bid valid for a shorter period shall be rejected, being non-responsive.

9. BID SUBMISSION

9.1 Instruction to Bidder

- I) Bidders are required to enrol on the e-Procurement module of the **Central Public Procurement Portal (URL: https://eprocure.gov.in/eprocure/app)** by clicking on the link "**Online Bidder Enrolment**" on the CPP Portal. **The registration is completely free of charge**.
- II) Possession of a valid Class II/III DSC in the form of smart card / e-token is a prerequisite for registration and participating in the bid submission activities. DSCs can be obtained from the authorised certifying agencies recognized by CCA India (e.g. Sify/TCS/nCode/eMudhra etc).

- III) Bidders are advised to register their valid email address and mobile numbers as part of the registration process. These would be used for any communication from the CPP Portal
- IV) Only one valid DSC should be registered by a bidder. Please note that the bidders are responsible to ensure that they do not lend their DSCs to others which may lead to misuse.
- V) The Bidders are required to log in to the site through the secured log-in by entering their respective user ID / password and the password of the DSC.
- VI) The CPP portal also has user manuals with detailed guidelines on enrolment and participation in the online bidding process. The user manuals can be downloaded for reference.

9.2 TENDER CLARIFICATION

- I) In case the bidders require any clarification regarding the tender documents, they are requested to contact our office Ph. no: 0877-2503572, Email ID: purchase@iittp.ac.in on or before due date.
- II) Technical and Specifications related Clarifications contact our office No: 0877 2503259 Email ID: prashanthy@iittp.ac.in on or before due date.
- III) Any queries relating to the process of online bid submission or queries relating to CPP Portal in general may be directed to the 24x7 CPP Portal Helpdesk.

9.3 ONLINE BID SUBMISSION PROCEDURE

Cover-1: The file should be saved in a PDF version numbered sequentially and should comprise of the following items:

Packet-1:

Duly Completed Scanned PDF copy of, PAN, GST, Firm Registration certificate and Annexure-I to VIII with relevant supporting documents

Only the relevant documents as per the tender clauses are to be uploaded along with duly completed checklist as per the annexure-IX. Uploading of other than the required documents may liable for rejection of the bid.

Cover-2:

A standard BOQ format has been provided in excel format. Bidders are required to download the BOQ excel file and fill their financial offer on the same BOQ format. After filling the same, submit it online in excel format, without changing the financial template format.

Note:

If the bid is incomplete and / or non-responsive it will be rejected during technical evaluation. The bidder may not be approached for clarifications during the technical evaluation. So, the bidders are requested to ensure that they provide all necessary details in the submitted bids.

10. BID OPENING

- 10.1 Technical Bids will be opened on **09.06.2022@ 15.00 Hrs.**
- 10.2 Financial Bids of the eligible bidders will be opened on a later date. The date and time for opening of Financial Bids will be announced later.
- 10.3 Bids should be summarily rejected, if tender is submitted other than through online or original tender fee/Bid security declaration are not submitted within stipulated date / time.

11. BID EVALUATION

Based on results of the Technical evaluation IIT Tirupati evaluates the Commercial Bid of those Bidders who gets qualify in the Technical evaluation. <u>The Commercial Bid with the lowest</u> price will be the highest evaluated bid.

11.1 Purchase Preference

I) Micro and Small Enterprises (MSEs):

Micro and Small Enterprises (MSEs) as defined in MSE Procurement Policy issued by Department of Micro, Small and Medium Enterprises (MSME) for goods produced and services rendered, may be provided following purchase preference:

Item wise Quantity	Price Quoted by MSE	How the tender shall be finalized
Cannot be split	L1	Full Order on MSE
Cannot be split	Not L1 but within L1 +	Full Order on MSE subject to matching L1
	15%	Price

II) Preference to Make in India

- a) In procurement goods or works which are covered under by para 3(b) of the extant Public Procurement (Preference to Make in India) Order 2017 dated 04 June 2020 and which are **divisible** in nature, the "Class-I Local Supplier" shall get purchase preference over "Class-II Local Supplier" as well as "Non-Local Supplier" as per following procedure:
 - i) Among all qualified bids, the lowest bid will be termed as L1. If L1 is "Class-I Local Supplier", the contract for full quantity will be awarded to L1.

- ii) If L1 bid is not a "Class-I Local Supplier", 50% of the order quantity shall be awarded to L1. Thereafter, the lowest bidder among the "Class-I Local Supplier" will be invited to match L1 price for the remaining 50% quantity subject to the Class-I Local Supplier's quoted price falling within the margin of L1 + 20%, and contract for that quantity shall be awarded to such "Class-I Local Supplier" subject to matching the L1 price. In case such lowest eligible "Class-I Local Supplier" fails to match L1 price or accepts less than the offered quantity, the next higher "Class-I Local Supplier" within the margin of L1 + 20% shall be invited to match the L1 price for remaining quantity and so on, and contract shall be awarded accordingly. In case some quantity is still left uncovered on Class-I local suppliers, then such quantity may be ordered on the L1 bidder.
- b) In procurement goods or works which are covered under by para 3(b) of the extant Public Procurement (Preference to Make in India) Order 2017 dated 04 June 2020 and which are **not divisible** in nature, and in procurement of services where the bid is evaluated on price alone, the "Class-I Local Supplier" shall get purchase preference over "Class-II Local Supplier" as well as "Non-Local Supplier" as per following procedure:
 - i) Among all qualified bids, the lowest bid will be termed as L1.

If L1 is "Class-I Local Supplier", the contract will be awarded to L1.

- ii) **If L1 is not a** "Class-I Local Supplier", the lowest bidder among the Class-I Local Supplier, will be invited to match the L1 price subject to Class-I Local Supplier's quoted price falling within the margin of L1 + 20%, the contract shall be awarded to such Class-I Supplier subject to matching the L1 price.
- iii)In case such lowest eligible Class-I Local Supplier fails to match the L1 price, the "Class-I Local Supplier" with the next higher bid within the margin of L1 + 20% shall be invited to match the L1 price and so on and contract shall be awarded accordingly. In case none of the of Class-I Local Supplier within the margin of L1 + 20%, the contract may be awarded to the L1 bidder.
- iv) Class-II Local Supplier will not get purchase preference.

12. PAYMENT TERMS

No advance payment will be made in any case. Bills in Duplicate should be sent and the payment shall be released generally within 30 days, only after it is ensured that the items /

quality of the items supplied are to the entire satisfaction of IIT Tirupati and completed the entire work within the stipulated delivery schedule. If any item is found defective, or not of the desired quality etc., the same should be replaced by the firm(s) immediately for which no extra payment shall be made.

13. WARRANTY OF QUALITY AND QUANTITY

- 13.1 The awardee shall give Minimum **3-years Onsite Warranty** on successful completion of supply, and acceptance of supplied items.
- 13.2 The awardee shall give warranty that all items are as per specification(s), conforming to the specified design and there are no defects in the process of manufacturing, packaging, transportation and delivery.
- 13.3 Upon receipt of notice from IIT Tirupati for defective material, the firm shall **within**15 days of receipt of the notice, replace the defective material, free of cost at the destination. The firm shall take over the defective material at the time of their replacement. No claim whatsoever shall lie on IIT Tirupati for the replaced goods thereafter. If the firm fails to replace the defective goods within a reasonable period, IIT Tirupati may proceed to take such remedial actions as may be necessary, at the company's risk and expense.

14. LIQUIDATED DAMAGES

In case of delay in Supply by the stipulated date, IIT Tirupati reserves the right of imposing penalty @0.5% per week on the value of the undelivered items subject to maximum 10% of the cost of undelivered items.

15. DELIVERY SCHEDULE

15.1 The successful bidder should execute the order successfully i.e. Supply, Installation of ordered item within **4 weeks** at IIT Tirupati transit campus, Venkatagiri Road, Yerpedu Post, Tirupati, Chittoor District from the date of issue of the purchase order. In case of any damage/Broken/Expired items found, the item(s) should be replaced within **15 days** at IIT Tirupati. The bidder has to make own arrangement for unloading and positioning of items at the desired location of IIT Tirupati.

16. PERFORMANCE SECURITY DETAILS

The successful tenderer will have to deposit the performance security valid for 39 Months in the form of DD / TDR / FDR / Bank Guarantee @ 03% of the total order value at the earliest from the date of issue of the award letter. No interest will be paid by IIT Tirupati on the deposit.

- Performance Security will be refunded to the supplier, after it duly performs and completes the contract/warranty period in all respects.
- 16.3 Performance Security will be forfeited if the firm fails to perform/abide by any of the terms or conditions of the contract.
- In case, the firm fails to execute the order successfully, within specified delivery period, the same goods/items will be procured from open market and the difference of cost, if any, will be recovered from Performance Security or from pending bill(s) of the defaulting firm or from both in case the recoverable amount exceeds the amount of Performance Security.

17. TERMS AND CONDITIONS

17.1 Termination for Insolvency

- The IIT Tirupati may at any time terminate the Contract by giving a written notice to the awarding firm, without compensation to the firm, if the firm becomes bankrupt or otherwise insolvent as declared by the competent Court, provided that such termination will not prejudice or affect any right of action or remedy, which has accrued or will accrue thereafter to the department.
- II) IIT Tirupati and/or the firm are entitled to withdraw/cancel the rate contract by serving one-month notice on each other. However, once a purchase order is placed on the supplier for supply of a definite quantity in terms of the rate contract during the validity of the rate contract, that purchase order becomes a valid and binding contract.
- III) The courts of Tirupati alone will have the jurisdiction to try any matter, dispute or reference between the parties arising out of this purchase. It is specifically agreed that no court outside and other than Tirupati Court shall have jurisdiction in the matter

17.2 Force Majeure

- I) Should any force majeure circumstances arise, each of the contracting parties be excused for the non-fulfilment or for the delayed fulfilment of any of its contractual obligations, if the affected party within 15 days of its occurrence informs in a written form the other party.
- II) Force Majeure shall mean fire, flood, natural disaster or other acts such as war, turmoil, sabotage, explosions, epidemics, quarantine restriction, strikes, and lockouts i.e. beyond the control of either party.

17.3 Arbitration

I) All disputes of any kind arising out in connection with the executing the order shall be referred by either party (IIT TIRUPATI or the bidder) after issuance of 30 days' notice in writing to the other party clearly mentioning the nature of dispute to a single arbitrator acceptable to both the parties. The venue for arbitration shall be IIT TIRUPATI India. The jurisdiction of the courts shall be Tirupati, Andhra Pradesh, India.

17.4 Other Conditions

- The bidder has to upload the relevant & readable files only as indicated in the tender documents. In case of any irrelevant or non-readable files, the bid may be rejected.
- II) IIT Tirupati will not be liable for any obligation or supplies made unless the Official Purchase Order has been placed by the Purchase Department.
- III) IIT Tirupati reserves the right to accept or reject any or all the tenders in part or in full or may cancel the tender, without assigning any reason thereof.
- IV) IIT Tirupati reserves the right to relax / amend / withdraw any of the terms and conditions contained in the Tender Document without assigning any reason thereof. Any inquiry after submission of the quotation will not be entertained.
- V) IIT Tirupati reserves the right to modify/change/delete/add any further terms and conditions prior to issue of purchase order.
- VI) In case the bidders/successful bidder(s) are found in breach of any condition(s) at any stage of the tender, Performance Security shall be forfeited.
- VII)False declaration/documents will be in breach of the Code of Integrity under Rule 175(1) (h) of the General Financial Rules for which a bidder or its successors can be debarred for up to two years as per Rule 151 (iii) of the General Financial Rules along with such other actions as may be permissible under law.
- VIII) Repeat Order: IIT Tirupati reserves the right to place repeat order up to 100% of the quantities within a period of 12 months from the date of successful completion of purchase order at the same rates and terms subject to the condition that there is no downward trend in prices.
 - To take care of any change in the requirement during the currency of the contract, a plus/minus option clause for 25 per cent is incorporated in the tender document, reserving purchaser's right to increase or decrease the quantity of the required goods up to that limit without any change in the terms and conditions and prices quoted by the tenderers.
- IX) Conditional tenders will not be considered in any case.
- X) In case of doubt in material, the expenditure on testing of equipment will be borne by the tenderer.
- XI) Institute reserve the right to increase/decrease the order quantity at any period of times during the validity of the contract.
- XII) IIT Tirupati may issue amendment/corrigendum to tender documents before due date of submission of bid. Any amendment/corrigendum to the

tender document if any, issued by IIT Tirupati will be posted on CPP Portal. For the bidders, submitting bids on downloaded tender document, it is 'bidders' responsibility to check for any amendment/corrigendum on the website of IIT Tirupati or check for the same CPP Portal before submitting their duly completed bids.

UNDERTAKING

To

The Registrar,

Indian Institute of Technology Tirupati-Renigunta Road, Settipalli post, Tirupati 517506.

Tender No. IITT/ ELE/2022-23/22 dated: 18 -05-2022.

Name of the Tender/Supply: Notice Inviting Tender for Supply, installation, testing and Commissioning of Data Acquisition System.

Sir,

I/we hereby submit our bid for Supply, installation, testing and Commissioning of Data Acquisition System.

I/ We enclosed here with the following in favor of Indian Institute of Technology Tirupati towards Tender Fee.

Particular	Amount	Payment Reference Details	Payment Date
Tender Fee (Including Tax)	500/-		

- 1. I / We hereby reconfirm and declare that I / We have carefully read, understood & complying the above referred tender document including instructions, terms & conditions, scope of work, schedule of quantities and all the contents stated therein. I / We also confirm that the rates quoted by me / us are inclusive of all taxes, duties etc., applicable as on date.
- 2. I/we have gone through all terms and conditions of the tender document before submitting the same.

Date: Place:		Authorized Signatory
	Seal	Name:
		Designation: Contact No:

On Company Letter Head

Bid Security Declaration

To

The Registrar,

Indian Institute of Technology Tirupati-Renigunta Road, Settipalli post, Tirupati 517506.

Tender No. IITT/ ELE/2022-23/22 dated: 18-05-2022.

Name of the Tender/Supply: Notice Inviting Tender for Supply, installation, testing and Commissioning of Data Acquisition System.

Sir,

We, the undersigned declare that

- 1. We understood that, according to the tender conditions, bids must be supported by a Bid Security Declaration.
- 2. We accept that we will automatically be suspended from being eligible for bidding in any contract with the Institute for the period of **3 years** starting from the bid closing date, if we are in breach of our obligation(s) under the bid conditions, because we;
 - (a) have withdrawn our bid during the period of bid validity specified in the letter of bid; or
 - (b) having been notified of the acceptance of our bid by the institute during the period of bid validity, (i) fail or refuse to execute the contract, if required, or (ii) fail or refuse to furnish the performance security, in accordance with the tender conditions.

Date: Place:		Authorized Signatory
	Seal	Name:
		Designation: Contact No :

CERTIFICATE (To be provided on letter head of the firm)

I hereby certify that the above firm is not in the active debarred list by any Central/State Government/Public Undertaking/Institute nor is any criminal case registered / pending against the firm or its owner / partners anywhere in India.

I also certify that the above information is true and correct in every respect and in any case at a later date it is found that any details provided above are incorrect, any contract given to the above firm may be summarily terminated and the firm may be blacklisted.

Date:		Authorized Signatory
Place:	Seal	Name:
riace:		Designation: Contact No.:

a) Experience: (As per tender Clause No.4.2 (III)

Year	Name of the Item with	Purchase Order	Date of successfully	Contact
	Specification (Technical specification	No. & Date (Copy of the Orders to	completion of SITC of ordered Item (copy of	Details of Client
	brochure to be	be attached)	Installation report from client	
	attached)		to be attached)	
2017-18				
2018-19				
2019-20				
2020-21				

b) Past Performance: (As per tender Clause No.4.2 (III)

Year	Purchase Order No. & Date (Copy of the Orders to be attached)	Quantity	Date of successfully completion of SITC of ordered Item (copy of report from client to be attached)	Whether supplied item(s) is in successful operation for at least one year (Certificate from client to be attached)	Contact Details of Client [email and phone no]
2017-18				,	
2018-19					
2019-20					
2020-21					

Date :		Authorized Signatory
Place:	Seal	Name: Designation:
		Contact No.:

ANNEXURE – V

Annual Turnover and Profit Details:

	Evalu	ation Criteria		Remark	Specific page no. where the proof of documents are enclosed
Bidder's Annual	Financial Year	Turnover in Rs.	Annual Profit in Rs.	-	
Turnover and Profit for last	2020-21			Supporting Documents are to be	
three financial	2019-20			attached along with the Annexure-V [i.e. Audited financial	
years	2018-19			Statements or Financial Statements showing turnover duly signed by a Chartered	
	2017-18			Accountant are to be submitted]	

Date:		Authorized Signatory: Name:
Place:	Seal	Designation:
riace.		Contact No.:

Format for Self-Declaration under preference to make in India order

In line with Government Public Procurement Order No. P-45021/2/2017-BE-II date. 15.06.2017 & P-45021/2/2017-PP (BE-II) dated: 04 June 2020. We hereby certify that we M/s (supplier name) are CLASS -
I/Class-II (Please specify clearly) supplier meeting the requirement of local content more than 20% as defined in above orders for the material against Enquiry No. IITT/ELE/2022-23/22 dated: 18-05-2022.
Details of location at which local value addition will be made as follows: (Complete address to be mentioned)
Percentage of Local Content:
(As per the OM of Department of Promotion for Industry and Internal Trade No. P-45021/102/2019-BE-II-Part(1) dated: 04.03.2021. The bidders can't claim themselves as Class-I local suppliers/Class-II local suppliers by claiming the services such as transportation, insurance, installation, commissioning, training and after sales service support like AMC/CMC etc. as local value addition)
We also understand, false declarations will be in breach of the Code of Integrity under rule 175 (1) (i) (h) of the General Financial Rules for which a bidder or its successors can be debarred for up to two years as per Rule 151 (iii) of the General Financial Rules along with such other actions as may be permissible under law.
Seal and signature of Supplier
Date :
Place :

Technical Compliance statement

	Description	Com	Remar	Offere	% of	Coun
	•	plied	ks, if	d	Local	try of
		(Yes/	any	Make	Content	Origi
		No)	•	&	as per	n
		,		Model	Tender	
					Clause	
					No.4.2(
					V)	
DATA ACQUISITI	ON SYSTEM -01 No.				• ,	
-	cations for the Data Acquisition System have					
been given below:	suitons for the Butter requisition by stem have					
been given below.	Number of channels 4 differential					
	ADC resolution 16 bits					
	DNL No missing codes					
	INL Refer to the AI Absolute Accuracy section.					
	Sample rate (simultaneous sampling on all					
	channels sampled)					
	Maximum 3.571 MS/s Minimum No minimum					
	Timing resolution 10 ns					
	Timing accuracy 50 ppm of sample rate Input					
	coupling DC					
	Input range ±1 V, ±2 V, ±5 V, ±10 V					
	Maximum working voltage for all analog inputs					
	Positive input (Al+) ±11 V for all ranges,					
	Measurement Category I					
	Negative input (AI-) ±11 V for all ranges,					
	Measurement Category I Caution Do not use for measurements within					
Analog Innut						
Analog Input	Categories II, III, and IV.					
	CMRR (at 60 Hz) 75 dB Bandwidth 1 MHz THD - 80 dBFS					
	Input impedance Device on					
	Al+ to Al GND >100 G Ω in parallel with 100 pF					
	Al- to Al GND >100 G Ω in parallel with 100 pl					
	pFDevice off					
	Al+ to Al GND 2 kΩ					
	Al- to Al GND 2 kΩ					
	Input bias current ±10 pA					
	Crosstalk (at 100 kHz) Adjacent channels -80					
	dB Non-adjacent channels -100 dB					
	Input FIFO size 8,182 samples shared among					
	channels used					
	Data transfers DMA (scatter-gather),					
	programmed I/O					
	Overvoltage protection for AI <03>, APFI 0					
	overvoitage protection for Al Vo37, Al 110					

		_	- 		- 			
	Device on ±36 V Device off ±15 V							
	Input current during overvoltage conditions	ĺ						
	±20 mA max/Al pin							
	Number of triggers 1							
	Source AI <03>, APFI 0 Functions Start							
	Trigger, Reference Trigger, Pause Trigger,							
	Sample Clock, Sample Clock Timebase							
	Source level							
	AI <03> ±Full scale							
	APFI 0 ±10 V							
	Resolution 16 bits							
	Modes Analog edge triggering, analog edge							
Analog Triggers	triggering							
Allalog Triggers	with hysteresis, and analog window triggering							
	Bandwidth (-3 dB)							
	AI <03> 3.4 MHz							
	APFI 0 3.9 MHz							
	Accuracy ±1% of range							
	APFI 0 characteristics							
	Input impedance 10 kΩ							
	Coupling DC		Ì					
	Protection, power on ±30 V							
	Protection, power off ±15 V							
	Gain tempco 8 ppm/°C							
Al Absolute Accuracy	Reference tempco 5 ppm/°C Residual offset							
(Warranted)	error 15 ppm of range							
	INL error 46 ppm of range							
	Number of channels 2							
	DAC resolution 16 bits							
	DNL ±1 LSB, max							
	Monotonicity 16 bit guaranteed							
	Accuracy Refer to the AO Absolute Accuracy							
	section Maximum update rate (simultaneous)							
	1 channel 3.3 MS/s							
	2 channels 3.3 MS/s							
	•							
	Minimum update rate No minimum							
	Timing accuracy 50 ppm of sample rate							
	Timing resolution 10 ns							
	Output range ±10 V, ±5 V, ±external reference							
Analog Output	on APFI 0							
	Output coupling DC		Ì					
	Output impedance 0.4 Ω		Ì					
	Output current drive ±5 mA							
	Overdrive protection ±25 V							
	Overdrive current 10 mA							
	Power-on state ±5 mV		Ì					
	Power-on/off glitch 1.5 V peak for 200 ms							
	Output FIFO size 8,191 samples shared among							
	channels used							
	Data transfers DMA (scatter-gather),							
			١					
	programmed I/O							
	AO waveform modes Non-periodic waveform,		Ì					

Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable	<u></u>	
regeneration from host buffer including dynamic update Settling time, full-scale step, 15 ppm (1 LSB) 2 μs Slew rate 20 V/μs Glitch energy at midscale transition, ±10 V range 6 nV · s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		·
dynamic update Settling time, full-scale step, 15 ppm (1 LSB) 2 μs Slew rate 20 V/μs Glitch energy at midscale transition, ±10 V range 6 nV · s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Settling time, full-scale step, 15 ppm (1 LSB) 2 μs Slew rate 20 V/μs Glitch energy at midscale transition, ±10 V range 6 nV·s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute Accuracy (Warranted) AO Absolute Accuracy (Warranted) AO Absolute Accuracy (Warranted) Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Do Sample Clock frequency Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many Al, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
μs Slew rate 20 V/μs Glitch energy at midscale transition, ±10 V range 6 nV·s		•
Slew rate 20 V/μs Glitch energy at midscale transition, ±10 V range 6 nV · s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute Accuracy (Warranted) AO Absolute Accuracy (Warranted) ASSUME accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/samples Waveform acquisition (DI) FIFO 2,047 samples Waveform acquisition (DI) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Do Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing output timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Glitch energy at midscale transition, ±10 V range 6 nV · s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform Characteristics (Port 0 Do Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Do Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, Do timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
range 6 nV·s APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Do Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
APFI 0 characteristics Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Only) Waveform Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Done Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		range 6 nV · s
Input impedance 10 kΩ Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Done Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		APFI 0 characteristics
External Reference Coupling DC Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples US ample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many Al, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
External Reference Protection, device on ±30 V Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 ON Sample Clock frequency Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many Al, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Protection, device off ± 15 V Range ±11 V Slew rate ±20 V/μs Absolute Accuracy (Warranted) AD Absolute Accuracy (AD Absolute Accuracy (PO Accura	External Reference	, -
Range ±11 V Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many Al, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Slew rate ±20 V/μs Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Only) Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, D0 timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Absolute accuracy at full-scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Do Sample Clock frequency Only) Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, D0 timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		-
AO Absolute Accuracy (Warranted) immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI < 07>/P1, PFI < 815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Usamples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		• •
assumes the device is operating within 10 °C of the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Waveform Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable	AO Absolute Accuracy	,
the last external calibration. Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Only) Waveform Eiro O to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable	•	
Static Characteristics Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable	(Warrantea)	
Number of channels 24 total, 8 (P0.<07>), 16 (PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
(PFI <07>/P1, PFI <815>/P2) Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Ground reference D GND Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Digital I/O/PFI Direction control Each terminal individually programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (D1) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		•
programmable as input or output Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable	Digital I/O/PFI	
Pull-down resistor 50 kΩ typical, 20 kΩ minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		-
minimum Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		
Input voltage protection ±20 V on up to two pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (D0) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		
pins Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		-
Terminals used Port 0 (P0.<07>) Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Port/sample size Up to 8 bits Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Waveform generation (DO) FIFO 2,047 samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		, ,
Samples Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Waveform acquisition (DI) FIFO 255 samples DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent DO Sample Clock frequency Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
DI Sample Clock frequency 0 to 10 MHz, system and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		•
System and bus activity dependent Characteristics (Port 0 Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		, , , , , , , , , , , , , , , , , , , ,
Characteristics (Port 0 DO Sample Clock frequency Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable	Maria farma	, , , , , , , , , , , , , , , , , , , ,
Only) Regenerate from FIFO 0 to 10 MHz Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Streaming from memory 0 to 10 MHz, system and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable	·	·
and bus activity dependent Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 µs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable	Only)	-
Data transfers DMA (scatter-gather), programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		, , ,
programmed I/O Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		, ,
Digital line filter settings 160 ns, 10.24 μs, 5.12 ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
ms, disable Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Functionality Static digital input, static digital output, timing input, timing output Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		
output, timing input, timing output Timing output sources Many Al, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		·
PFI/Port 1/Port 2 Functionality Timing output sources Many AI, AO, counter, DI, DO timing signals Debounce filter settings 90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable		
Functionality DI, DO timing signals Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable		output, timing input, timing output
Functionality Debounce filter settings 90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable	DEI/Dort 1/Dort 2	Timing output sources Many AI, AO, counter,
ms, custom interval, disable; programmable	•	DI, DO timing signals
	runctionality	Debounce filter settings 90 ns, 5.12 μs, 2.56
high and low transitions: selectable per input		ms, custom interval, disable; programmable
		high and low transitions; selectable per input

		_	- ,	 	, , , , , , , , , , , , , , , , , , , 	 	<u> </u>
	Input high voltage (VIH)						
	Minimum 2.2 V						
	Maximum 5.25 V						
	Input low voltage (VIL)						
	Minimum 0 V						
Recommended	Maximum 0.8 V						
Operating Conditions	Output high current (IOH)						
	P0.<07> -24 mA maximum						
	PFI <015>/P1/P2 -16 mA maximum						
	Output low current (IOL)						
	P0.<07> 24 mA maximum						
	PFI <015>/P1/P2 16 mA maximum						
	Positive-going threshold (VT+) 2.2 V maximum						
	Negative-going threshold (VT-) 0.8 V minimum						
Digital I/O	Delta VT hysteresis (VT+ - VT-) 0.2 V minimum						
Characteristics	IIL input low current (VIN = 0 V) -10 μA						
Characteristics	maximum						
	IIH input high current (VIN = 5 V) 250 μΑ						
	maximum						
	Number of counter/timers 4						
	Resolution 32 bits Counter measurements						
	Edge counting, pulse, pulse width, semiperiod,						
	period, two-edge separation						
	Position measurements X1, X2, X4 quadrature						
	encoding with Channel Z reloading; two-pulse						
	encoding						
	Output applications Pulse, pulse train with						
	dynamic updates, frequency division,						
	equivalent time sampling						
Timing I/O	Internal base clocks 100 MHz, 20 MHz, 100 kHz						
	External base clock frequency 0 MHz to 25						
	MHz						
	Base clock accuracy 50 ppm						
	Inputs Gate, Source, HW_Arm, Aux, A, B, Z,						
	Up_Down, Sample Clock						
	Routing options for inputs Any PFI, RTSI,						
	analog trigger, many internal signals						
	FIFO 127 samples per counter						
	Data transfers Dedicated scatter-gather DMA						
	controller for each counter/timer,						
	programmed I/O						
	Number of channels 1						
	Base clocks 20 MHz, 10 MHz, 100 kHz						
Frequency Generator	Divisors 1 to 16						
	Base clock accuracy 50 ppm						
	Number of PLLs 1 Output of PLL 100 MHz						
Phase-Locked Loop	Timebase; other signals derived from						
(PLL)	100 MHz Timebase including 20 MHz and						
\(\frac{1}{2}\)	100 kHz Timebases						
<u> </u>	TOO KIIZ TIIIICDUSES						

	Source Any PFI, RTSI
	Polarity Software-selectable for most signals
	Analog input function Start Trigger, Reference
	Trigger, Pause Trigger, Sample Clock, Convert
	Clock, Sample Clock Timebase
	Analog output function Start Trigger, Pause
	Trigger, Sample Clock, Sample Clock Timebase
External Digital	Counter/timer functions Gate, Source,
Triggers	HW_Arm, Aux, A, B, Z, Up_Down, Sample
00	Clock
	Digital waveform generation (DO) function
	Start Trigger, Pause Trigger, Sample Clock,
	Sample Clock Timebase
	Digital waveform acquisition (DI) function Start
	Trigger, Reference Trigger, Pause Trigger,
	Sample Clock, Sample Clock Timebase
	Input source RTSI <07>
	Output destination RTSI <07>
	Output selections 10 MHz Clock, frequency
Device-to-Device	generator output; many internal signals
Trigger Bus	Debounce filter settings 90 ns, 5.12 μs, 2.56
	ms, custom interval, disable; programmable
	high and low transitions; selectable per input
	Form factor x4 PCI Express, specification v1.1
	compliant
Bus Interface	Slot compatibility x4, x8, and x16 PCI Express
	slots
	DMA channels 7 DMA, analog output, digital
	input, digital output, counter/timer 0,
	counter/ timer 1, counter/timer 2,
	counter/timer 3
Power Requirements	3.3 V 4.0 W and 12 V 13.2 W
	5 V terminal (connector 0) 1 A maximum2
Current Limits	PO/P1/P2/PFI terminals combined 1.4 A
	maximum
	Printed circuit board dimensions 16.8 cm ×
	11.1 cm (6.60 in. × 4.38 in.)
	Weight 110 g (4.0 oz)
	I/O connectors
n	PCIe device connector 68-Pos Right Angle
Physical	Single Stack PCB-Mount VHDCI (Receptacle)
	Cable connector 68-Pos Offset IDC Cable
	Connector (Plug) (SHC68-*) Form factor
	Standard height, half length, single slot
	Integrated air mover (fan) No
Calibration	Recommended warm-up time 15 minutes
	Calibration interval 2 years
Safety Voltages	Channel-to-earth ground ±11 V, Measurement Category I
	Maximum altitude 2,000 m (800 mbar) (at 25
Environmental	°C ambient temperature)
LIIVII OIIIIIEIILAI	Pollution degree 2
	Poliution degree 2

	Operating temperature, local 0 °C to 50 °C			
Operating	Operating humidity 10% to 90% RH,			
Environment	noncondensing			
	System slot airflow 0.4 m/s (80 LFM)			
	Ambient temperature range -20 °C to 70 °C			
Storage Environment	Relative humidity range 5% to 95% RH,			
Required Accessories	noncondensing			
	SCB-68A Noise Rejecting, Shielded I/O			
	Connector Block -1Quantity SHC68-68-EPM			
	Shielded Cable, 68-D-Type to 68 VHDCI Offset,			
Required Accessories	2 m BNC-2110 Noise Rejecting, Shielded BNC			
	Connector Block -1Quantity			
	And All required accessories.			
Warranty	Three Years Onsite warranty.			
Spares and Service support Availability	Minimum 5 years			

COMPANY DETAILS

Date of Incornoration /		
Date of Incorporation / Registration details		
PAN Number		
GST Registration Number		
Bidder's Bidding Capacity for the tendered items (As a Manufacturer/ Trader/ dealer / channel partner / system integrator, etc.)		
	Account Number	
	IFS Code	
Bank Details	Bank Name	
	Branch Name	
Registered Office Address		
Authorized Signatory Details	Name	
	Name Designation	
(Company/Firm Authorization		
	Designation	
(Company/Firm Authorization by the competent authority, to	Designation Email	
(Company/Firm Authorization by the competent authority, to	Designation Email Phone	
(Company/Firm Authorization by the competent authority, to be attached)	Designation Email Phone Name	
(Company/Firm Authorization by the competent authority, to be attached) Details of Contact other than	Designation Email Phone Name Designation	
(Company/Firm Authorization by the competent authority, to be attached) Details of Contact other than	Designation Email Phone Name Designation Email	Signature and Seal of the Tendere
(Company/Firm Authorization by the competent authority, to be attached) Details of Contact other than Authorized Signatory	Designation Email Phone Name Designation Email	Signature and Seal of the Tendere Name in Block Letter:

Contact no.

ANNEXURE-IX

CHECKLIST FOR BIDDERS TO BE SUBMITTED IN DULY FILLED AND SIGNED

Tender Clause	Name of the Document	Document	Submitted	Page No. of
No.		Particulars	(Yes/No)	the attached Document
3.1	Tender Fee			Document
3.4	Bid security Declaration (Annexure-II)			
3.3	Valid Tender Fee / EMD Exemption Certificate			
4.1.	PAN Card			
	Incorporation/Registration certificate of company			
	GST Registration copy			
4.2.(I)	Tender acceptance letter (Annexure I)			
4.2.(II)	Non-Blacklisting undertaking (Annexure III)			
4.2.(III)	The bidder/OEM should have supplied similar			
	system during past three financial years i.e. during			
	2017-18 to 2019-20 or 2018-19 to 2020-21 in India to Central / State Govt/ PSU/ CPSEs/ Educational			
	R&D Institutions. Vendor should provide satisfactory			
	installation certificates with product details as proof			
	with customer contacts email and phone number as			
	per the Annexure-IV .			
4.2.(IV)	The Annual Turnover should be at least Rs. 1 Lakh			
	and be profitable during each of the previous three			
	financial years i.e. during 2017-18 to 2019-20 or			
	2018-19 to 2020-21. Audited financial Statements or			
	Financial Statements showing turnover duly signed by			
	a Chartered Accountant are to be submitted as per the			
	Annexure-V.			
4.2.(V)	The bidder should be a <u>Class-I/Class</u> in line with the			
1.2.()	Public Procurement (Preference to Make in India)			
	Order 2017 No. P-45021/2/2017-PP (BE-II) dated 04			
	` '			
	Jun 2020. A Self-Declaration Certificate regarding			
	"Class-I & Class-II Supplier" for the tendered items as			
4.0 (7.11)	per the Annexure-VI is to be submitted.			
4.2.(VI)	The bidder should be OEM or OEM authorized			
	Dealers / Channel partners / Distributors of reputed			
	brand having authorization for sales and after sales			
	support. Valid OEM authorization letter is required to			
	participate in this tender.			
4.2.(VII)	Any bidder from a country which shares a land border			
	with India will be eligible to bid in this tender only if			
	the bidder registered with the competent authority.			
	The concerned bidder(s) are required to attach the			
	relevant valid Registration Certificate along with the bid for consideration.			
4.3	Technical Compliance Statement : Annexure-VII.			
7.3	recinical Comphanice Statement . Annexure-vII.		1	

11.1 (I)	Purchase Preference: (if applicable)		
	Micro and Small Enterprises (MSEs):		
11.2 (II)	Purchase Preference: Make in India		
12	Payment Term: Within 30 days after SITC.		
13.	Onsite Warranty: 3 Years onsite warranty		
2.1	Spares and service support: Minimum 5 years from		
	the date of supply		
15	Delivery: FOR IIT Tirupati within 4 weeks		
8	Bid validity: 90 days from the date of opening of the		
	tender		
	Company details : Annexure-VIII		

Note:

- 1) Submission of tender without the above mentioned documents will lead to rejection/disqualification of the tender.
- 2) It is mandatary for the bidder to assign page numbers to the tender documents and the same has to be mentioned in the above checklist.

Signature of the bidder with stamp